2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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TC 2800 MAIL ROOM

Applicant: Leonard Forbes et al.

Title: DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Docket No.: 303.586US1
Filed: May 26, 1999
Examiner: Anh-Quan Tra

Serial No.: 09/320,421
Due Date: February 8, 2001
Group Art Unit: 2816

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response (8 Pages).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 8th day of February, 2001.

Amy Moriarty
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(GENERAL)

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#16/Resp 2/16/01 Sunler

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AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on November 8, 2000. Please amend the above-identified patent application as follows.

IN THE DRAWINGS

The drawings were objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the dual-gated transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

As explained in more detail below in connection with the 102 discussion, Figures 2A and 3 of the Applicant's drawing set illustrate a pair of "dual-gated" transistors. One of the pair is represented as M3, M5, and the other one of the pair is shown as M4, M6. There is no conventional circuit symbol for a "dual-gated" or "double-gated" MOSFET of the type used in the Applicant's invention. Applicant, thus must create its own representation. Accordingly, each one of the pair of "dual-gated" transistors is illustrated with a box-like structure, which represents a single body region. The single body region has gates on opposing sides of the single body region. This structure is distinguishable from the a conventional dual gate MESFET, having dual gates only on one side of a single body region, and is distinguishable from a schematic illustration of MOSFETs connected in parallel, which is also described and sketched below for reference in connection with the 102 discussion.

IN THE SPECIFICATION

The specification was objected to as being misdescriptive. The Examiner states:

> Page 10, line 16-30, describes the pair of transistors M3, M5 and M4, M6 of each inverter, B1 and B2, comprises a dual-gated MOSFET. It is well known in the art that a dual-gated transistor is